INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40106B gates
Hex inverting Schmitt trigger

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

DESCRIPTION

Each circuit of the HEF40106B functions as an inverter with Schmitt-trigger action. The Schmitt-trigger switches at different points for the positive and negative-going input signals. The difference between the positive-going voltage (V_P) and the negative-going voltage (V_N) is defined as hysteresis voltage (V_H).

This device may be used for enhanced noise immunity or to "square up" slowly changing waveforms.

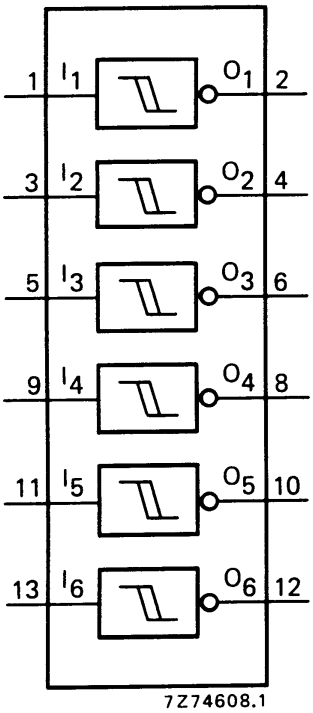

Fig.1 Functional diagram.

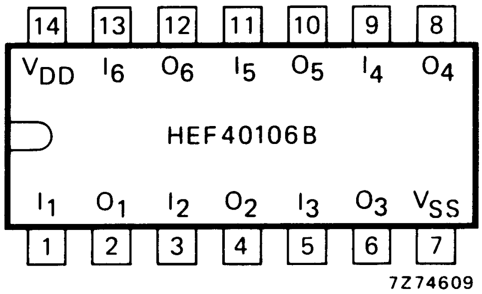

Fig.2 Pinning diagram.

HEF40106BP(N): 14-lead DIL; plastic (SOT27-1)

HEF40106BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

HEF40106BT(D): 14-lead SO; plastic (SOT108-1)

( ): Package Designator North America

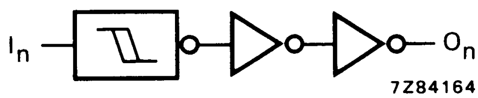

Fig.3 Logic diagram (one inverter).

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

DC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Hysteresis	5		0,5	0,8		V
voltage	10	V_H	0,7	1,3		V
	15		0,9	1,8		V
Switching levels	5		2	3,0	3,5	V
positive-going	10	V_P	3,7	5,8	7	V
input voltage	15		4,9	8,3	11	V
negative-going	5		1,5	2,2	3	V
input voltage	10	V_N	3	4,5	6,3	V
	15		4	6,5	10,1	V

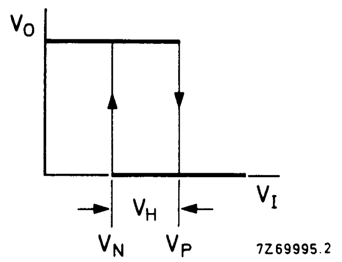

Fig.4 Transfer characteristic.

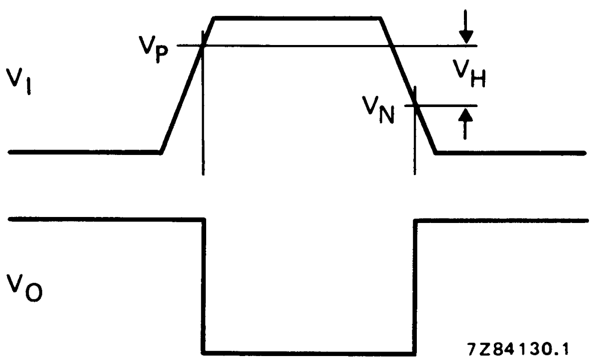

Fig.5 Waveforms showing definition of V_P, V_N and V_H, where V_N and V_P are between limits of 30% and 70%.

AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \rightarrow O_n$	5		90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF)
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		75	150	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$2\,300\ f_i + \sum (f_oC_L) \times V_{DD}^2$	where
dissipation per	10	$9\,000\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$20\,000\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_oC_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

Hex inverting Schmitt trigger

HEF40106B gates

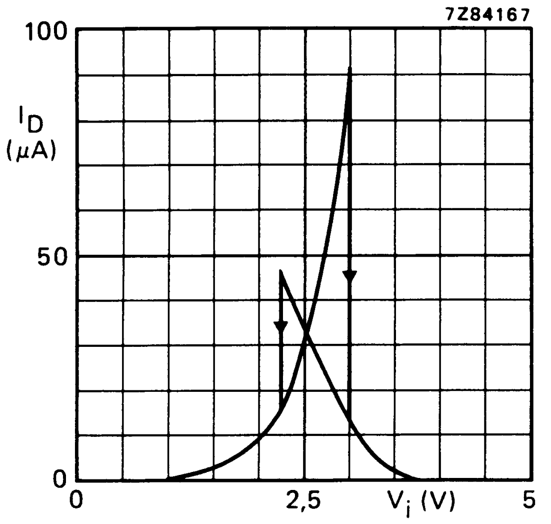

Fig.6 Typical drain current as a function of input voltage; V_{DD} = 5 V; T_{amb} = 25 °C.

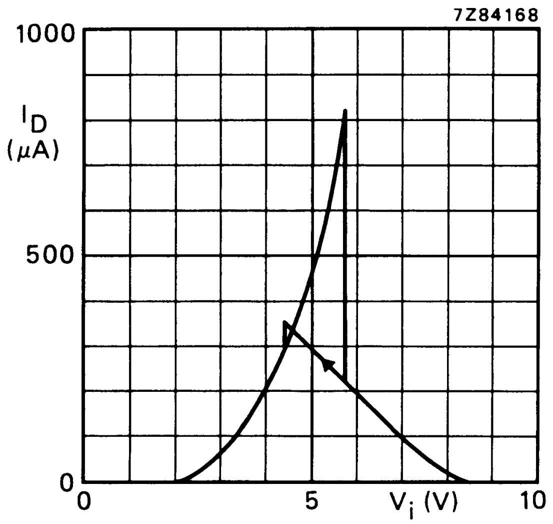

Fig.7 Typical drain current as a function of input voltage; V_{DD} =10 V; T_{amb} = 25 °C.

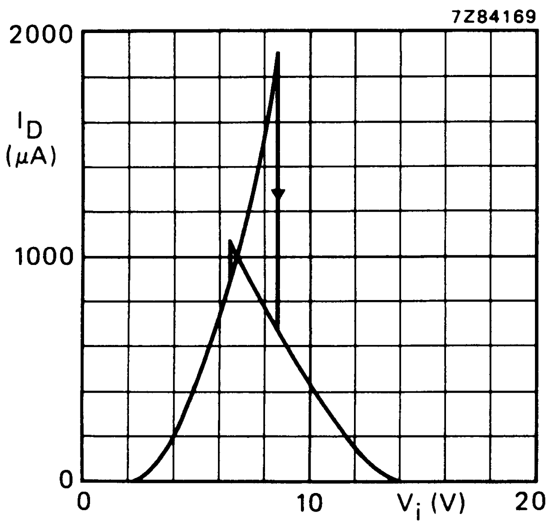

Fig.8 Typical drain current as a function of input voltage; V_{DD} = 15 V; T_{amb} = 25 °C.

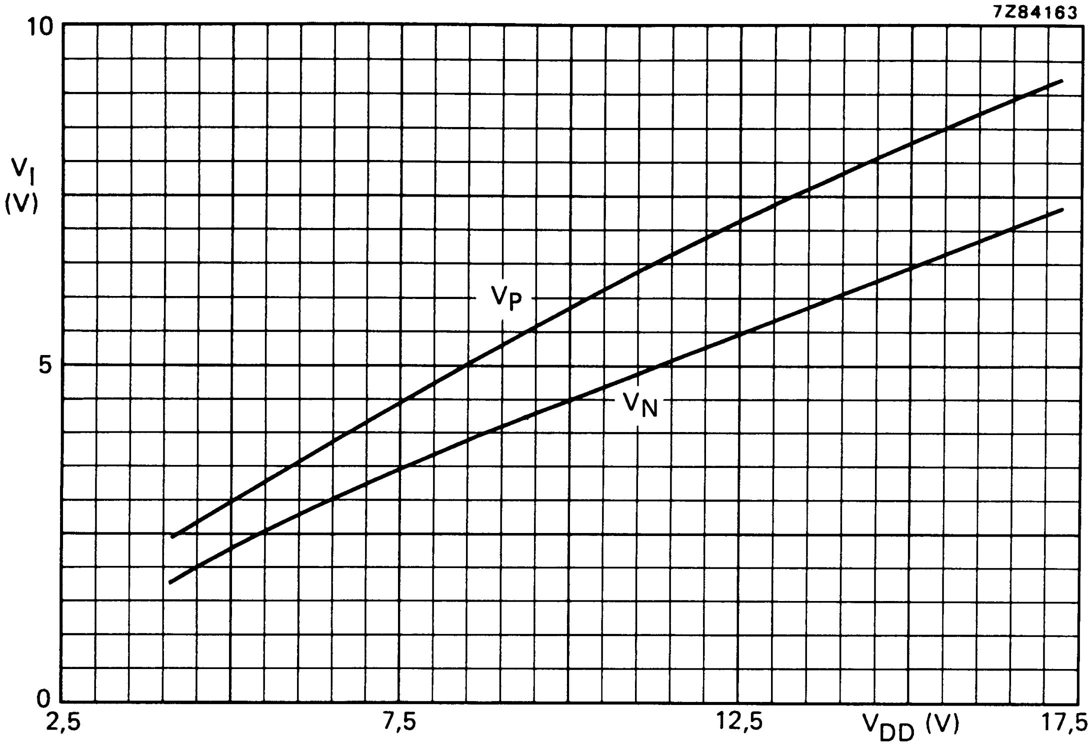

Fig.9 Typical switching levels as a function of supply voltage V_{DD}; T_{amb} = 25 °C.

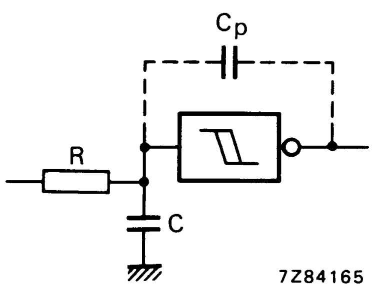

Fig.10 Schmitt trigger driven via a high impedance (R > 1 kΩ).

If a Schmitt trigger is driven via a high impedance (R > 1 kΩ) then it is necessary to incorporate a capacitor C of such value that: $\frac{C}{C_p} > \frac{V_{DD} - V_{SS}}{V_H}$, otherwise oscillation can occur on the edges of a pulse.

C_p is the external parasitic capacitance between input and output; the value depends on the circuit board layout.

APPLICATION INFORMATION

Some examples of applications for the HEF40106B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

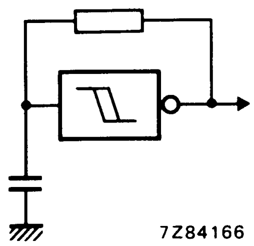

Fig.11 The HEF40106B used as an astable multivibrator.