

TECHNICAL REPORT

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AUTHORS	: S.Venkataramanan, Arti Gupta
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NUCLEAR SCIENCE CENTRE

(An Autonomous Inter-University Centre of UGC)

Post Box No.: 10502, Aruna Asaf Ali Marg,

New Delhi 110067 (India) Phone: 2689 3955, 2689 2603, 2689 2601

Fax: 091-11-2689 3666

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Prepared by

**ELECTRONICS LABORATORY
NUCLEAR SCIENCE CENTRE,
P.B.10502,
NEW DELHI 110067.**

Technical Report on Charge Sensitive Preamplifier (NSCPAC1-SBD)

S.Venkataramanan¹, Arti Gupta²
Electronics Laboratory, Nuclear Science Centre,
P.B.10502, Aruna Asaf Ali Marg,
New Delhi 110067
^{1,2}email: venkat@nsc.ernet.in, arti@nsc.ernet.in

Abstract

A general purpose high density Charge Sensitive Preamplifier for use with silicon surface barrier detector has been developed and implemented successfully at NSC. The low noise wide bandwidth amplifier with programmable open loop gain is implemented with state of the art low noise SMT devices. A fast "TIMING" information is provided for TOF experiments.

Acknowledgment

We would also like to acknowledge the efforts put-up by Detector Lab peronnels at NSC during evaluation and would like to thank Dr. Amit Roy and Ajith Kumar. B.P. for their constant encouragement and providing the necessary infrastructure in order to complete this project successfully.

Specifications

Charge Sensitive Preamplifier

Rise time

NSCPAC1 (with JFET)	Detector Capacitance	
	0 pF	156 pF
U310	14ns	54ns
IF1331	16ns	84ns
Dual BFW10	15ns	160ns
2N5486	16ns	230ns
2N4416A	16ns	260ns
BFW10	16ns	320ns

Canberra Preamp (model 2003T)	9ns	20ns
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Ortec preamp (model 142A)	9ns	32ns
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Noise (keV, Si)

NSCPAC1 (with JFET)	Detector Capacitance	
	0 pF	156 pF
U310	4.35keV	7.75keV
IF1331	4.44keV	7.43keV
Dual BFW10	4.46keV	10.22keV
2N5486	4.37keV	10.57keV
2N4416A	4.42keV	11.37keV
BFW10	4.51keV	12.64keV

Canberra Preamp (model 2003T)	2.19keV	3.22keV
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Ortec preamp (model 142A)	2.56keV	5.08keV
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Open Loop Gain	~90dB for U310 & IF1331
Charge Sensitivity (Si, equivalent)	44mV/MeV (optional)
Energy Range	0 - 200 MeV (optional)
Decay Time	100 μ s
Detector Bias Voltage	+/- 1KV maximum
Connectors	SHV- 1704 for Detector bias LEMO- 00 for other Inputs and Outputs
Power required	+/-12V/ 40 mA through LEMO connector
Cabinet	Die-cast Aluminium case.

Introduction

A high density charge-sensitive preamplifier is developed to use with SSB detector. It provides both Energy and Time outputs for amplitude and timing measurements respectively.

Noise in charge-sensitive preamplifier depends on the input FET and total input capacitance, contributed by input cable, detector capacitance and feedback capacitor C_f . In our preamplifier C_f is chosen for the sensitivity of 44mV/MeV. To minimize the noise due to input cable, preamplifier should be placed within the specified distance from the detector. Noise performance of preamplifier was analyzed for detector capacitance in the range of 10 to 150 pF using various FETs i.e. IF1331, U310, single and dual BFW10, 2N5486 & 2N4416A. The performance of the preamplifier, using best FETs, was also compared with the commercial preamplifiers 142A (EG&G ORTEC) and 2003T (Canberra) and graphs are plotted for the same.

Principle of operation

The input stage of the preamplifier consists of a FET amplifier, a current amplifier and a transresistance amplifier, using Op-Amp AD829, in closed loop with a RC network. The value of the RC time constant decides the decay time of the Energy output pulse. AD829JR is a low noise video amplifier (1) with external compensation capacitor, which can be adjusted to get the best rise time of the Energy output.

Energy output pulse polarity is inverted from the signal polarity at the detector output while timing output has the same polarity as that of the detector output. However the polarity of the energy output can be changed by using on-board-jumpers.

Preamplifier output stage consists of a wide band gain stage in composite with buffer amplifier. The operational amplifier LM6171, chosen for gain stage, is a high speed, wide bandwidth, unity gain stable video amplifier (2) and BUF_634 is high dynamic range, wide bandwidth buffer amplifier. These two stages are in composite configuration (3) to achieve wide good bandwidth, dynamic range and low dc offset. Energy output dc offset can be adjusted by a multiturn pot mounted on the PCB. Output impedance of Energy output is $\sim 50\Omega$.

Operating bias for the detector is supplied to the SHV connector. Through a filter and large bias resistor it goes to the input signal connector. From there it is furnished out through the signal input cable to the detector.

Preamplifier Energy output rise time and noise varies with the detector capacitance. To record this a test pulse from the pulser such as ORTEC 419 is given to the Test input ($Z_{in}=100\Omega$) and detector equivalent capacitor is connected at the detector input. The shape of this pulse should be a fast rise time(<10ns) followed by a slow exponential decay back to the baseline (200 to 400 μ s). A series capacitor of 1pF at the Test input converts the applied voltage into equivalent charge.

Timing output (50 Ω termination) gives better than 10ns rise time irrespective of change in FET and detector capacitance. However best rise time we got with pulser is 2ns. To get the best timing performance preamplifier should be placed within 30cm distance from the detector.

The DC power supply lines are dc coupled with solid tantalum and ceramic chip capacitors. Also the power supply lines are protected against accidental reversal of supply lines. The circuit is realized with surface mount components like high quality ceramic chip capacitors and metal film resistors.

Test Results

Energy output rise time and noise performances of the preamplifier were analyzed for detector capacitance in the range of 10 to 150 pF with different FETs (IF1331, U310, single and dual BFW10, 2N5486 & 2N4416A). It was observed that owing to high transconductance i.e. g_m , IF1331 & U310 give best performance in terms of noise (eV/pF) and energy output rise time (ns/pF). The performance of the preamplifier using these two FETs was also compared with the commercial preamplifiers 142A (EG&G ORTEC) and 2003T (Canberra) and graphs are plotted for the same (Fig1 to 4).

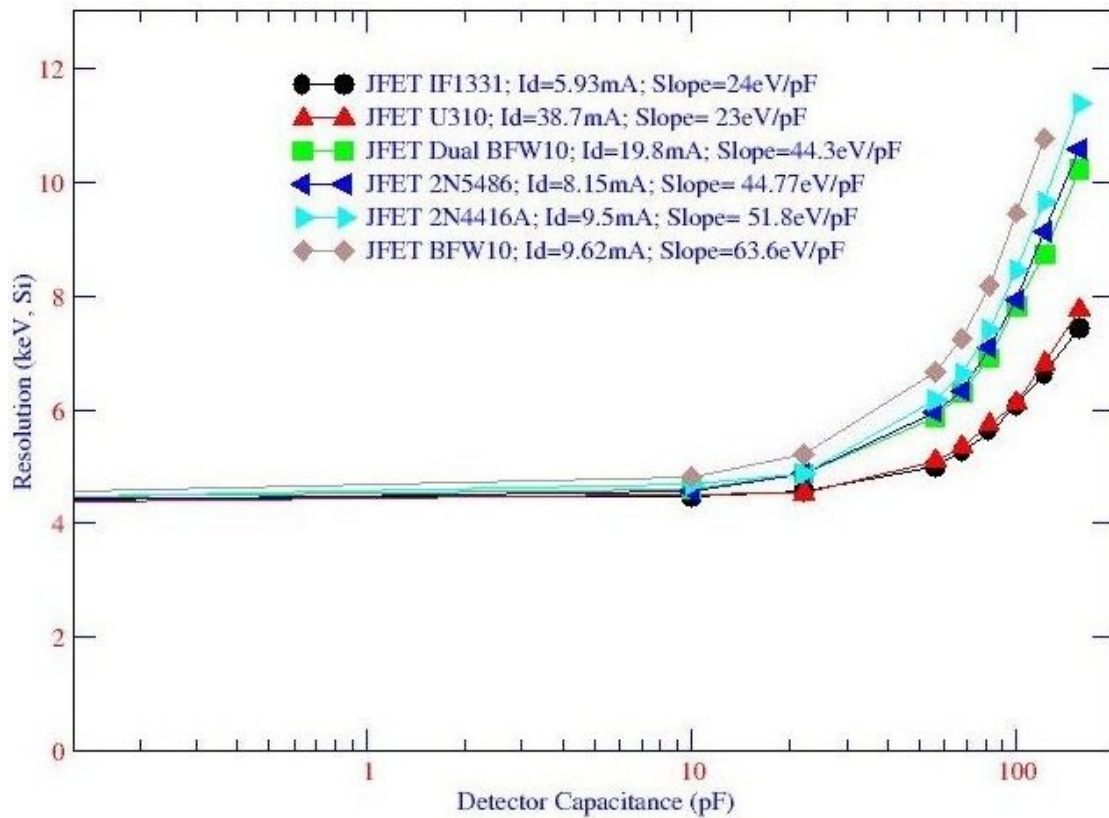


Fig 1: NSCPAC1- Energy Characterization using different FETs
(Pulser EG&G 419, Ortec 572 Amp:2uS, URE-3 RMS/Noise meter,
Si equ: 44mV/MeV)

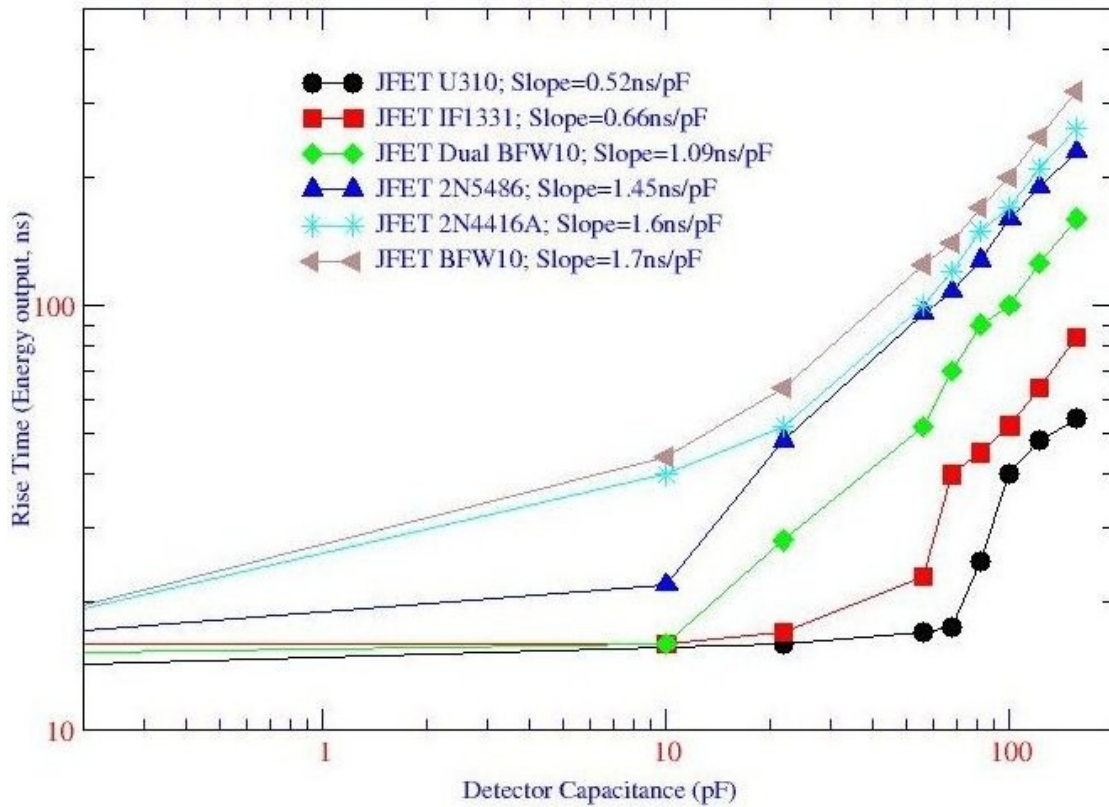


Fig 2: NSCPAC1- Energy output Rise time Characterization using different JFETs (Pulser EG&G 419, Ortec 572 Amp:2uS, URE-3 RMS/Noise meter, Si equ: 44mV/MeV)

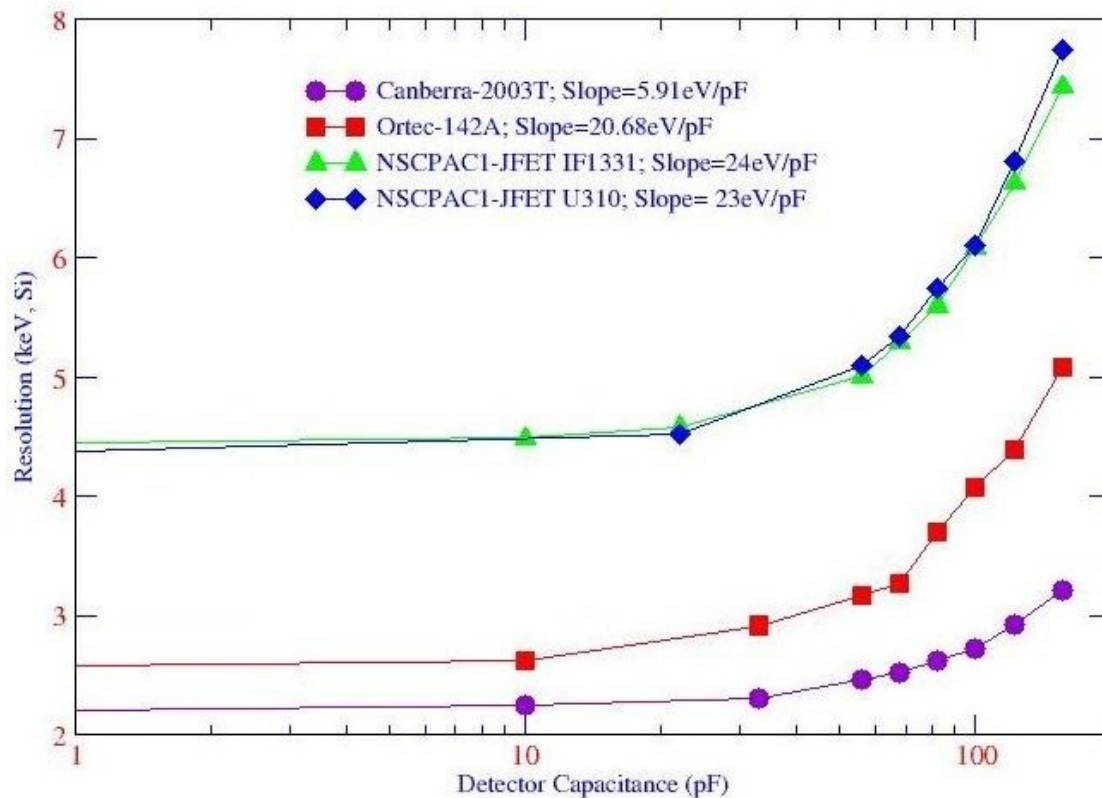


Fig 3: Energy Characterization of NSCPAC1, EG&G 142A and Canberra 2003T Preamplifiers.

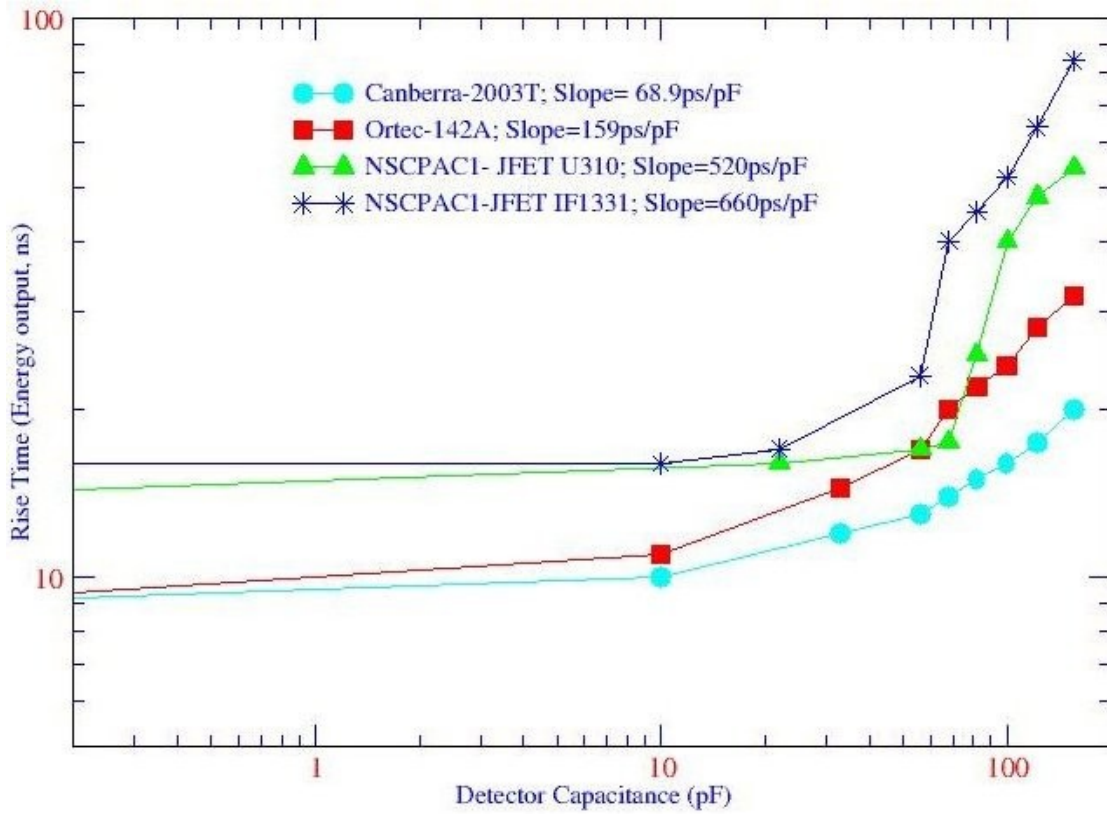


Fig 4: Energy output Rise time Characterization of NSCPAC1, EG&G 142A and Canberra 2003T Preamplifiers.

Assembly Procedure

The currently available PCB is of glass epoxy, double sided with 0.6mm drill PTH having dimension of 3.5" x 1.5" with all above features.

It is recommended to have solder mask and silk screen printed on both sides for easy assembly as well to protect it from solder bridges etc.,. Use of 0.8mm sharp solder tip, IC solder tips are recommended in order to solder narrowly spaced SMT devices. SMT devices shall be picked only by fine quality tweezers. While soldering a magnifier x5 (large) and x12 (eye piece) is used to assure the soldering. It is essential to use solder cleaning liquid with cotton swab to remove dust attracting solder paste.

The PCB shall be checked with magnifiers and multimeter for any unwanted connections and PTHs. Then components shall be soldered in a orderly manner, to start with all low profile chip resistors and capacitors. It is essential to check the impedance between various nodes after soldering resistors, capacitors and inductors. Active components like diodes, transistors and ICS are soldered thereafter. At last tantalum capacitors, connectors, jumpers and any non-SMT devices. All PCBs shall be marked distinctly with unique number for any future references.

Conclusion

A high density Charge sensitive preamplifier unit is successfully developed and tested.

References

1. AD829 data sheet. <http://www.analog.com>
2. LM6171 data sheet <http://national.com>
2. Application bulletin on "Combining an Amplifier with the BUF634" by Burr Brown. <http://ti.com>

