VMEDAC64 12-bit 64 Channel DAC for VMEbus

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Abstract

A new VMEDAC64, a Versa Module Europa (VME) module, features 64 Analog Voltage Outputs, has been developed for control applications at Inter University Accelerator centre (IUAC) on a 6U VMEbus. The FPGA (Field Programmable Gate Array) is the module's core; it implements the complexity of control logic and VMEbus slave interface. The low cost per channel or high density of 64 Analog Outputs on a single width 6U VME board is the unique feature of VMEDAC64 module which is not available in similar products at present. VME slave is implemented as a component in the firmware which can be used in the future designs without any change and hence speed up the prototyping. Control of analog output is as easy as writing the binary equivalent to a dedicated dual port register (per channel). Digital-to-analog conversion takes place automatically with total 7.040 ms (max.) output refresh time for 64 channels. Each channel has software controlled output switch which disconnects analog output from the field. The VMEbus slave interface and control logic is implemented in a single FPGA chip to achieve a density of 64 channels in a single width, double height (6U) VME module. On-board DC/DC converters are incorporated for isolated power supply requirements.

INTRODUCTION

The VMEDAC64 is a 64-Channel, 12-bit analog output board designed to operate in a standard VMEbus system. The board contains a 12-bit Digital-to-Analog Converter (DAC), dedicated onboard dual-port registers to store the output data, sample and hold buffers (S&H) and analog switches to place the voltage on the cable. There is a single 12-bit multiplying DAC chip which service all the 64 channels with multiple onboard precision references selected by REF_SEL[2:0] bits of Control and Status Register (CSR) to select the appropriate output range. Each output has a 12-bit resolution and a software programmable output range (0 to +5V, 0 to +10V, ±2.5V, ±5V, ±10V) and output refresh rate.

The module has jumper selectable output polarity i.e. unipolar or bipolar output. The analog output equivalent digital data is placed in the dual-port memory by the controlling processor through the VME port. The Digital-to-Analog conversion is controlled by the refresh control logic. This circuitry will periodically transfer digital data from dual port memory's refresh port to the DAC. Simultaneously the control logic connects the DAC output to the appropriate analog output de-multiplexer (analog distributor section). Each analog output has its own sample-and-hold buffers and a control switch and therefore receives an update once every 7.040ms in the default refresh mode. A program-controlled "FAST REFRESH" control bit, in the CSR, can be used to reduce the refresh cycle time to approximately 3.52ms, thereby double the output sampling rate from 142Hz to 284Hz. In both the refresh modes the output settling time of the DAC is kept same for each channel i.e. 10us.

The board control logic and dual-port memory is implemented in a single Field Programmable Gate Array (FPGA). The VMEbus slave interface of the VMEDAC64 module is compliant with the VMEbus specification[1]. It supports standard addressing data transfer capabilities and configurable interrupt level. The VMEbus interface signals are routed to FPGA through buffer chips. Buffer chips are generally used on the VMEbus interface because FPGA target devices usually do not have compatible inputs and outputs. VMEbus is based on TTL interface standards.

Figure 1: VMEDAC64 module inserted in VME crate.

GENERAL DESCRIPTION

The block diagram in Fig. 2 illustrates the overview of the board design. The 64 analog outputs in multiple software controlled output range are available on the front panel connectors. Since each analog output has a dedicated sample and hold buffer therefore each one is capable of driving 10mA of drive current. The main functional catagories described in Fig. 2 are :

- VMEbus Slave Interface Logic
- Analog Outputs (DAC and Analog Distributor)
- Analog Output Buffers and Switch

- Dual-Port Data RAM and Output Refresh Control Logic
- Power Converter

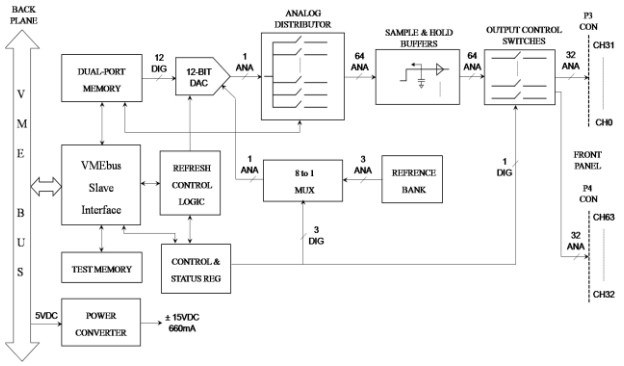

Fig. 2 Block diagram of VMEDAC64 module

VMEbus Slave Interface using FPGA

The VME core design is an A24:D16:D08(EO) interface, meaning that it participates in 24-bit addressing cycles and 16-bit (or smaller) data cycles[1]. The core design of VME responds to VMEbus single read and single write cycles. It also responds to the block transfer BLT16. We have implemented the design on Xilinx's Spartan IIE FPGA. The FPGA code is written as industry standard Hardware Description Language (VHDL).

Analog Outputs (DAC and Analog Distributor)

All 64 analog outputs are serviced by a single 12-bit multiplying Digital-to-Analog (DAC) converter. Each analog output has a dedicated sample and hold buffer and control switch to place voltage on the front panel output connector. The analog distributor consists of the following components :

- A one of 64 output channel decoder
- Low charge injection analog demultiplexer
- 64 capacitive storage elements and buffers

The timing sequence for the dual port memory access and the corresponding sample-and-hold buffer selection is shown in the Fig 3.

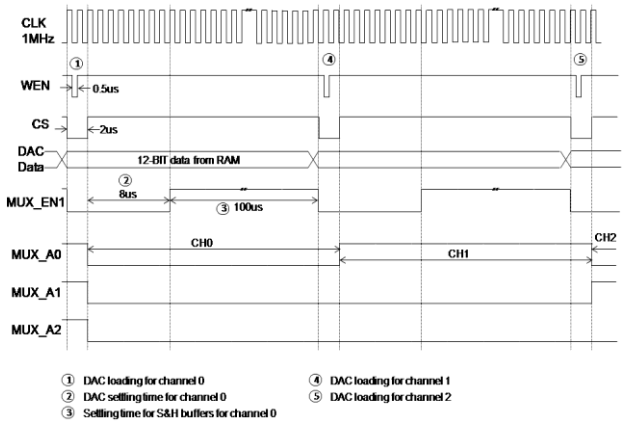

Fig. 3 Timing Diagram of the control signals for DAC and Analog Distributor section

Analog Output Buffers and Switches

The DAC converted voltage levels, processed by the analog distributor section and stored by the sample-and-hold storage capacitors, are buffered and then switched to the front panel connectors for routing through the system I/O cables. The output buffers are low leakage, precision operational amplifiers which can supply 10mA of drive current over full available output voltage range i.e. ±10V. The output switches are control by the OUTPUT ENABLE bit of the CSR register. These buffers can sustain short circuits to ground without damage.

Dual-Port RAM and Refresh Control Logic

The dual-port memory which services the analog outputs is organized as a 16-bit wide 64-column array and is implemented inside FPGA. Dual-port means either of the two ports can access each location. The random access VME port is used by the VME host to 'write' the analog output digital codes into the memory and the DAC port is used by the refresh control logic to 'read' analog output data for Digital-to-Analog conversion . The digital codes are then transferred sequentially through the DAC port to the Digital-to-Analog Converter. There they are converted into voltage levels and subsequently distributed to the appropriate analog output channel.

On-Board DC-DC Power Converter

The analog section of the VMEDAC64 module receives its electrical power from two on-board compact DC-DC power converters. The power converters transform the +5V logic power into isolated and regulated ±15VDC power, with a load capacity of 660mA on each 15V power line.

CONCLUSIONS

The VMEDAC64 module with 64 analog outputs and 12-bit resolution has been developed successfully at IUAC. This research centre has a tandem and LINAC ion beam accelerator and has PC based distributed control system [3] based on CAMAC standard with more than 500 parameters to control. The VMEbus slave interface along with interrupter and Block Transfer (BLT16) capabilities can be used as a basic building block for any VME module [2].

REFERENCES

[1] *VME Bus Specification VITA*, ANSI/IEEE Standard 1014-1987, 1987.

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[3] B.P. Ajith Kumar, E.T. Subrahmaniam and Kundan Singh, " Distributed control system for NSC tandem-LINAC," in *Indian Journal of Pure and Applied Physicst.*, vol. 39, pp. 1-3, Jan-Feb 2001.