HOME MADE FPGA BASED INSTRUMENTATION DEVELOPMENT FOR LINAC AUTOMATION AT IUAC

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Abstract

In order to make the Inter-University Accelerator Centre (IUAC) linac operation with less human intervention and with minimum effort, different mechanisms of automation are being thought of and are being implemented. Among the various projects in the automation, the first one is the development of a 16-channel digital linearizer unit for RF power read-backs and control. In another development, 8 channel programmable pulse generators (PPG) were designed, developed and used at the time of RF pulse conditioning of the SC resonators. As a third project of linac automation, a computer controlled drive probe controller was developed to control the movement of 8 drive couplers of the resonator along with position sensor read back mechanisms.

INTRODUCTION

The Superconducting booster linac project [1] at Inter University Accelerator Centre (IUAC) is presently working successfully along with the existing Pelletron control system to deliver the accelerated beam from the first superconducting linac module to the users. Improvement of the linac control scheme [2] is undertaken for automation with minimum human intervention during beam acceleration [3]. Some instrumentation has been developed in-house to cut down the costs. RF Power read back devices with linear voltage outputs, Simultaneous pulse conditioner for multiple resonators etc. are made possible by using dedicated hardware interfaced with standard CAMAC module and Python based client interface. Movement of the drive coupler is enabled from operation console with position read back. These modules have been successfully tested in the first LINAC cryostat.

RF READBACK & LINEARIZER UNIT

This FPGA based instrument accepts sixteen non-linear, low magnitude voltage inputs of the order of 0-10V proportional to RF forward and reflected powers of the superconducting resonators and are digitized to display all the 16 power readouts on a 40 * 4 character display. The device multiplexes the analog inputs using analog switches and produces linearized output voltage corresponding to each channel through 12 bit DACs. The linearization is done by piece-wise linear interpolation technique using VHDL to fit within an accuracy of +/- 0.5 W and display resolution 0.1 W. RS232 interface is implemented inside FPGA for PC based data logging. The linear output voltage of 0-10Vdc is used for CAMAC readbacks for main control applications. Figure 1 shows the block diagram of 16 channel linearizer unit.

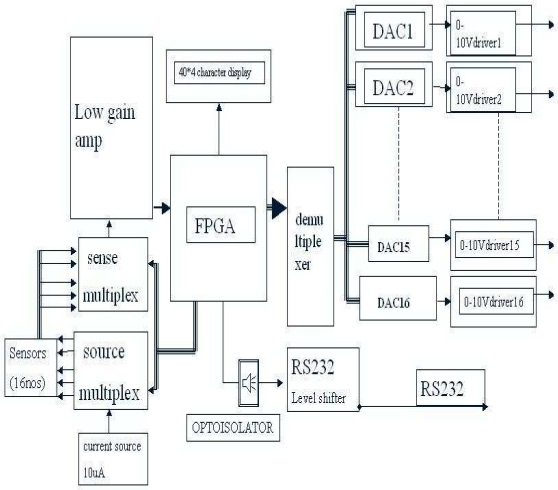

Figure 1: Block diagram of 16 channel linearizer unit.

PROGRAMMABLE PULSE GENERATOR

Since there are eight resonators in each accelerating module of linac, an eight channel programmable pulse generator has been designed as a single unit for the simultaneous high power conditioning of all the resonators. This device has 16 independent programmable interval registers, each individually programmable through CAMAC to produce 8 independent pulse streams. This device finds its use in high power RF pulse conditioning of all the eight resonators simultaneously by controlling the resonator control modules. The 40*4 display in the front-panel displays the stored programmed pulse durations, programmed from a computer through CAMAC. User sets the ON and OFF time individually from 1 millisecond to 4000 milliseconds. The output pulses are driven through 50 ohm driver circuits. Another single channel programmable pulse generator with a shaft encoder knob interface, is also developed for simple test cryostat facility for manual operations. This device also generates a pulse stream from 1 ms to 4000 ms and the ON/OFF time is displayed on a 16*2 VFD display. Fig.2 shows the logic diagram of a single channel PPG.

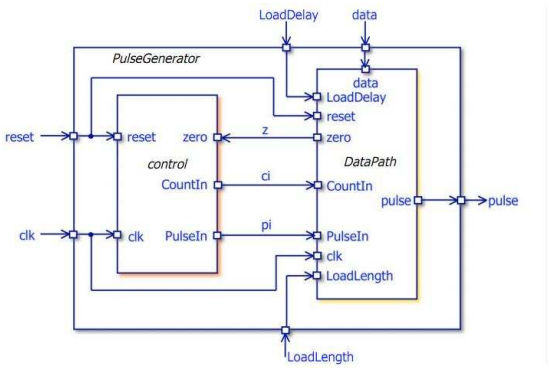

Figure 2: Logic diagram of single channel PPG.

POSITION READBACK & DRIVE PROBE CONTROLLER

An eight channel drive probe controller has been developed to move all eight drive probes to couple the RF power into the cavities. To show the actual position of drive probe, a position readout mechanism of the drive couplers has also been implemented using linear potentiometers as position sensors, displayed on a 8 channel display unit and on control computer. This device can be controlled from CAMAC based control system for their inward/outward movements. The straight line equation of all position sensors has been implemented inside FPGA to read back the positions in percentage on a 40*4 character display. An eight channel CAMAC analog to digital converter has been used to interface the 0 to 10 V dc output used for its position read back at the main control room. Fig.3 shows the position sensor assembly along with the display unit.

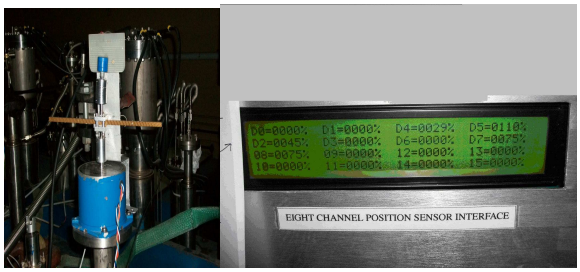

Figure 3: Drive probe position sensor readout system.

SUMMARY

All the above mentioned devices were indigenously developed by using the FPGA technology and are built around the chip Xilinx-4010E. The VHDL has been used to program the chip. All the above mentioned devices are provided with additional RS232 interfaces for local data logging if necessary. The quality of potentiometers used as position sensors is not very satisfactory as the pots exhibit noticeable non linearity in between its movements. Additionally it was noticed that the backlash error caused by the drive probes by virtue of its mechanical construction caused poor reproducibility of its absolute position between repeated movements.

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