ANALYSIS AND DESIGN OF HIGH POWER SOLID-STATE MODULE AT 350 MHZ FOR RF ACCELERATOR

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Abstract

Solid-sate power amplifier module using a high power LDMOS transistor has been analyzed and designed. Its performance matrices like power gain, power output, efficiency, and input and output match have been studied. Parametric analysis has been carried with respect to variation of matching elements. The design has been optimised for a power gain of >18 dB and a power output of 800 watts. The design is implemented on FR-4 substrate. Experimental results have been presented.

INTRODUCTION

A project has been proposed in the XIth plan to develop a high power solid-state amplifier for RF accelerators at BARC, Mumbai. Based on the earlier experience on development of solid state amplifiers [1] an attempt has been made to push the power limits per module beyond 300 watts. The solid-state power amplifier has several advantages over the vacuum tube amplifiers. These are mainly low cost, simple start-up procedure, long life, easy maintenance, low voltage power supplies, low power circulators, and high volume density etc.[2]. As per the recent studies on solid-sate power amplifiers, under proper thermal conditions, mean time between the failures (MTBF) of amplifiers is beyond 100 years. The performances of current LDMOS technologies like power gain, output power, efficiency etc are very much competent to vacuum tube amplifiers.

DESIGN OF MODULE

To design a high power solid-state module an LDMOS device, MRF6V41KH of Free scale semiconductor make is chosen. It has a power gain of 20 dB and an efficiency of 66% over a frequency range of 50-500 MHz [3]. The data sheet mentions that the device is mainly usable for pulse, 1KW application. But it also suggested the possibility using the same device for 1 kW, CW power output with liquid cooling.

The non-linear model of the device, MET model has been used in the analysis. The schematic circuit of the amplifier is shown in Fig. 1. The amplifier is in push-pull configuration. It uses two baluns B1 and B2 at input and output matching networks respectively. These are semi-rigid lines with characteristic impedance, Z_0 of 50 ohms. The lengths of these lines are chosen at 90 mm. A two section L-type matching networks are used for both input and output matching networks. These networks transfer the device impedances' to 25 ohms. These networks consist of coupled micro strip lines T1-T4 and shunt capacitors C1-C4. The capacitors, C5-C8 are coupling capacitors. Quarter wave lines, T6 & T7 with Z0, 50 ohm feed the drain bias and a resistive divider feed the gate bias. V_G and V_D are gate and drain bias supplies. The device is biased at V_{DS}, 50 V and I_D, 150 mA.

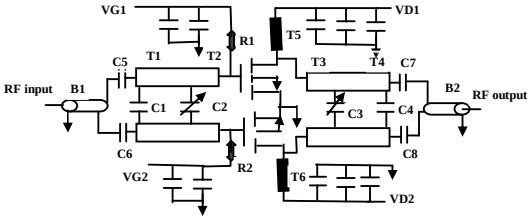


Figure.1 Schematic circuit of the amplifier.

Simulated Results

The circuit has been optimised with respect to network elements for a maximum gain and power output at 350 MHz. Optimised power gain and input match are shown in Fig. 2. It has a maximum gain of 18.8 dB and input return loss of 14.8 dB at 350 MHz.

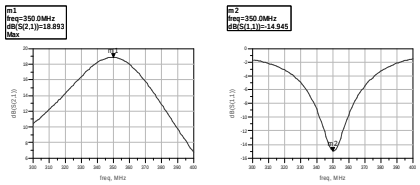


Figure 2: Simulated gain and input return loss.

TEST SET-UP

The test set-up of the power amplifier is shown in Fig. 3. It consists of a signal generator, SMB of R&S, a drive amplifier A1, two directional couplers C1 and C2, and two NRT power meters along with their power sensors.

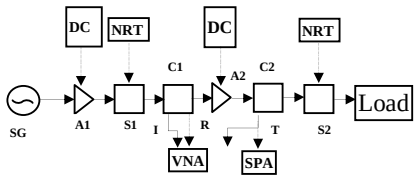


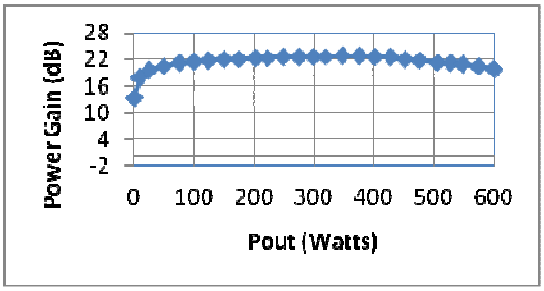
Figure 3: Measurement set-up.

The Test amplifier, A2 is terminated in to a 1 kW load. The vector network analyser (VNA) and spectrum analyser (SPA) are used to characterise the power amplifier. The drive amplifier A1 is a broadband amplifier

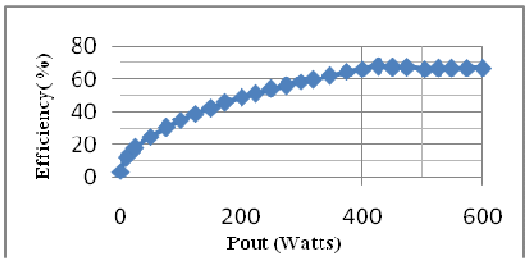
with a gain flatness of +/- 0.5 dB and a power gain of 48 dB over a frequency band of 200-500 MHz. The couplers C1 and C2 have coupling coefficient of 63 dB and directivity of >25 dB. The VNA is used in receiver mode. The signal ratio, T to I is used to measure the gain and phase response. The signal ratio R to I is used to measure the input match, S11 of the amplifier. The signal T is also used to measure the harmonics in SPA.

RESULTS

Measured results of the amplifier are shown in Fig.4. Fig. 4 (a) shows the power output versus power gain. At power output of 500 watts, the gain compression is >2 dB. This is mainly due to unequal drive between two devices. One device is operating at saturation. As per the temperature measurements on drain leads by an infrared thermo meter, upper device is over driven whereas lower device is less driven. Drain lead of upper the device is going up to 90 deg C. To correct this drive imbalance two variable capacitors have been connected between gates and ground and tuned. After correcting gate imbalance, the amplifier has been tested to a power output of 600 W with a gain of 20 dB. Fig. 4 (b) shows the Dc to RF conversion efficiency at different output power level. At low power levels <200 watts, efficiency of this amplifier is <50%. But at higher power level efficiency of the amplifier is >65%. Tested Power amplifier is shown in Fig. 5.



(a)



(b)

Figure 4: Performance data of power amplifier at 350 MHz (a) Power Gain vs. Output Power and (b) Efficiency vs. Output power.

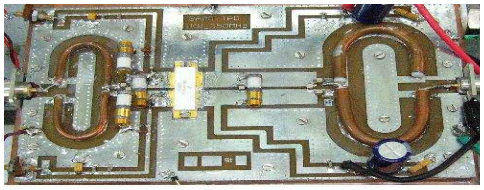


Figure 5: Tested power amplifier.

CONCLUSIONS

RF accelerators it is preferable to develop a special purpose power amplifier which has high power gain, high power output, and high conversion efficiency to minimise the number of power modules for particular application. It also reduces the heat load on ambient environment.

In Table 1, a comparison of specifications is made between this development and earlier developments.

Table 1: Amplifiers Comparison

Specs.	**LR301 [2]**	**DMD1029 [2]**	**This module**
Pout (W)	300	330	600
Gain (dB)	13	13	20
Efficiency (%)	65	60	64

The heat plate on which the device is mounted is clamped to water cooled Copper channel. This two layer sink made high thermal resistance and it lead to a drain temperature rise to 85 deg. To avoid any abnormal breakdown of devices, tests have been stopped. At 600 W device has been successfully operated for 4 fours. High power tests 800-1000 W is planned with direct mounting of device to a water cooled channel.

This type of solid-state module can be usable in future high power amplifiers for RF accelerators.

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