# DESIGN AND DEVELOPMENT OF A PULSE POWER SUPPLY FOR TESTING OF PULSE QUADRUPOLE MAGNET FOR 10MeV DRIFT TUBE LINAC

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#### Abstract

A project on injection linac for spallation neutron source has been taken up at RRCAT. The linac (H<sup>-</sup> ion) includes a 352 MHz drift tube linac (DTL) to accelerate a pulsed proton beam from 3 MeV to 10 MeV. In the DTL structure a pulsed electromagnetic quadrupole magnet is embedded in each drift tube for focusing the H<sup>-</sup> ion beam. The quadrupole magnet gradient will vary from 60 T/m to 40 T/m. The Quadrupole magnet will be operated at 25 Hz repetition rate. A prototype quadrupole magnet of 60 T/m magnetic gradient at 150A has been developed at RRCAT. To measure the field quality and field gradient of quadrupole magnet a pulse field measurement set up has been developed at RRCAT [3]. A pulse power supply to excite the quadrupole magnet for pulse field measurement set up has been designed and a prototype power supply has been fabricated and tested. This supply produces a pulse that is approximately a half sine wave with a base width of approximately 1.3ms; its peak current is adjustable form 50A to 250A. The flattop time of the pulse is >10 $\mu$ s. In the flat regime of current the tolerances is  $\pm 0.05\%$ of peak current.

#### **INTRODUCTION**

The pulse field measurement of a quadrupole magnet requires a current pulse to excite the quadrupole magnet. The requirements of current pulse can be met with a sine pulse. This is accomplished by discharging the energy stored in a capacitor bank into the magnet as illustrated by figure1. A dc power supply is used to charge the capacitor bank through an inductor to the required voltage. On triggering the forward thyristor S3 the energy stored in capacitor bank C1 is discharged into the magnet circuit Lm. S3 turns off at the end of the first half cycle of the damped oscillation. C1 is then left with a smaller charge of opposite polarity until the diode connected in anti parallel with forward thyristor S3 conducts and the second half cycle takes place with current flowing in the opposite direction. The difference between original and the final charge is furnished by the charging supply.

## **OPERATION**

### **Discharging** Circuit

The discharge circuit consists of C1, S3 and Lm in figure 1. When the capacitor bank, C1 is discharged into the load, by triggering thyristor S3, an oscillatory



Figure 1: Schematic diagram

current will result provided that the total resistance in the circuit is sufficiently low. The peak value of current is given by

Ip = Ec1 (C1/Lm)<sup>0.5</sup> e-((
$$\pi$$
Rm/4)(C1/Lm)<sup>0.5</sup>) (1)

After first half cycle of sinusoidal oscillation thyristor, S3 turns off and the voltage on the capacitor bank, C1 becomes reverse, at this time a diode, D1 connected in anti parallel becomes forward bias and a reverse current flows through circuit Lm, D1and C1. The capacitor bank is now charged to some positive potential.

#### Controlled Charging Circuit

The controlled charging circuit consists of L1, C1, S1, and S2 and a dc supply E. Triggering of S1 is used to start the charging of C1 from the dc power supply. At time t0 the supply voltage E begins sinusoidal current through the charging circuit. Applying KVL to charging circuit gives

 $E = iR1+L1 (di/dt) + (1/C) \int ic1dt$ At time t1 the current is at its peak and L1di/dt = 0, then

$$E=iR1+(1/C) \int ic1dt$$

Between t1 and t2 the decaying charging current generates a voltage L1 (di/dt) which aids the supply voltage to charge the capacitor C1 to a voltage larger than E. In case R1=0, this voltage will be, at time t2

$$Ec1=E+L (di/dt)=2E$$
(2)

The charging cycle can be terminated at any instant between time t1 and t2 by providing a thyristor across the charging inductor. A reference voltage is compared with a fraction of the capacitor bank voltage. When fraction of Ec1>= reference voltage, a pulse is generated to trigger the thyristor S3. With S3 conducting, the driving voltage L1 (di/dt) is removed from the circuit and the capacitor voltage Ec1 becomes larger than supply voltage. Thyristor S1 is back biased and the charging current stops. The current through inductor L1 will decay with a time constant L1/R, where R is the resistance of choke, L1, and thyristor, S2, circuit. By controlling the capacitor bank voltage required output peak current pulse can be obtained.



Figure 2: Quadrupole magnet pulse field measurement setup. Inset Quadrupole magnet





The charging components consists of L1=10mH, C1=  $240\mu$ F, S1 and S2 (50RIA120) and a dc power supply E and discharging components consists of C1, S3 (50RIA120) and Lm =  $875\mu$ H. Fig.3 shows charging voltage of capacitor bank and charging current through inductor L1 when the charging supply voltage is 200V.The charging cycle terminates between time t1 and t2. Fig 4 shows the capacitor bank voltage Ec1, inductor current IL1, and magnet current ILm during charging and discharging cycle. Fig. 5 shows the capacitor bank voltage and output current pulse during discharging the capacitor bank.



Figure 4: Charge and discharge cycle, Ec1, ILm and IL1.



Figure 5: Ec1 and ILm during discharging cycle.

## CONCLUSION

A pulse power supply for quadrupole magnet has been designed, assembled and tested in the laboratory. The stability of current pulse is found  $\pm 0.05\%$ . Using this power supply, pulse field measurement of a prototype Q-pole magnet has been done. The results of pulse field measurement agree with the theoretical data.

## ACKNOLEDGEMENT

We are grateful to Shri Y.P.Singh who helped us in the development of the power supply. Authors wish to thank Shri Surendra Veer for wiring and fabrication of various parts of power supply. We also thank Dr. P.D.Gupta, Director RRCAT for their constant support & encouragement

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