DESIGN AND DEVELOPMENT OF PCI EXPRESS DIGITAL I/O INTERFACE CARD

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Abstract

The paper discusses development of an 8 lane PCI Express digital I/O interface card, which can be used for variety of applications requiring high speed data transfer to PC. This new serial bus lane-wise architecture with scalability has many advantages over conventional parallel PCI bus. Applications requiring low speed can use only one lane of PCI Express wherein applications requiring high speed can use 2, 4, 8, 16 or 32 lanes of PCI Express depending on the speed requirement. Each serial lane of PCI Express has data transfer speed of 2.5 Giga bits per second and is duplex (can communicate in two directions simultaneously). This next generation bus does not define physical layer due to which data transfer can take place using copper wire or optical cables.

The 8 lane interface card uses Virtex-5 series of FPGA for implementing the PCI Express protocol. The interface card is a 16 layer PCB with proper impedance control for the PCI Express differential signals. The maximum data transfer speed of this card is 20 Giga bits per second and can be used for applications like high speed data acquisition, PXI Express 3U size module development etc. These applications are extensively used for Accelerator data acquisition systems as well as RF cavity controls.

PCI EXPRESS PROTOCOL

Figure 1 gives us the comparative information of various bus protocols. Needless to say that PCI Express bus protocol is the fastest with highest throughput achieved. The PC bus architecture is completely changed after introduction of PCI Express bus.

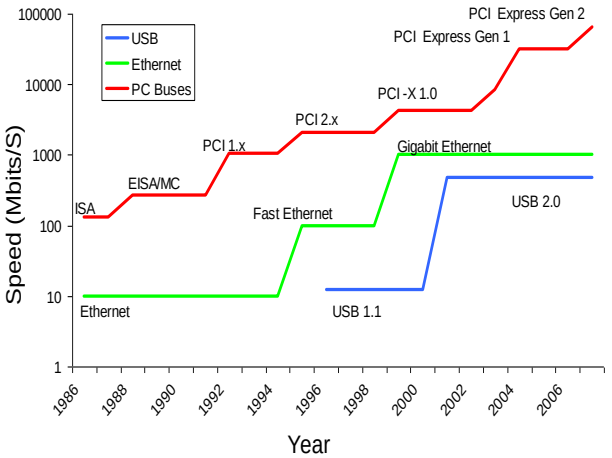

Figure 1: Comparison of various bus protocols

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Each device on a PCI Express bus has a dedicated PCI Express lane which is not shared with any other device. This unique ability (called as scalability) helps in increasing the overall system throughput by choosing the number of lanes (choice can be done in multiple of two like 2, 4, 8, 16 or 32 lanes) according to required bandwidth. Each lane can transmit data bi-directionally at 2.5 Gbps (Giga bits per second) and hence the combined data transfer rate achieved for an 8 lane PCI Express card is 20 Gbps in each direction simultaneously. Since the PCI Express protocol encodes each data byte using 8B/10B encoding scheme, the actual data which can be transmitted/received is 20% less than the theoretical speed of each lane. Hence actual data transfer speed of 8 lanes PCI Express card is 16 Gbps bi-directionally. It will reduce further when data is converted into packets.

Figure 2 shows the layered architecture of PCI Express protocol. The upper layers of software drivers and OS (Operating System) are the same as that of PCI bus. This reduces the burden of software designers for integrating the PCI Express device with the OS. The change is in the data format/integrity protocol wherein data is arranged as packets and each packet has address information and parity information added in the subsequent layers of the protocol. Also, that the data itself is encoded with 8B/10B encoding scheme for dc balance over transmitting lines. The physical layer of the PCI Express protocol is nothing but point-to-point connection between two points using differential pair. Each lane uses two differential pairs (one for transmitter and other for receiver). The media used for this connection is chosen by the user. It can be a copper pair used in motherboards or can be fibre optic cable connecting two systems. The data packet is transmitted/received on these differential pairs.

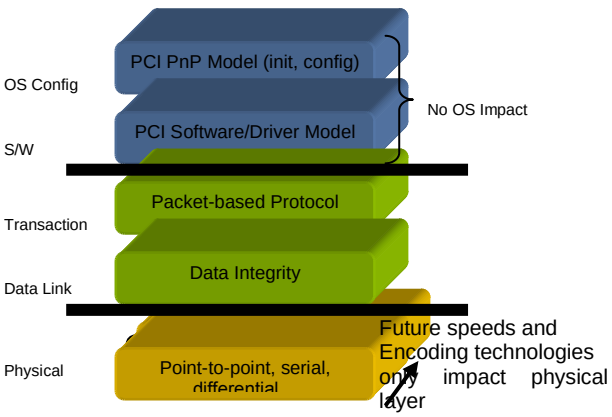

Figure 2: PCI Express layered architecture

BLOCK DIAGRAM DESCRIPTION

Figure 3 shows the basic block diagram of the PCI Express Interface card. The PCI Express protocol is implemented using Virtex-5 FPGA, which has inbuilt 'hard block' for PCI Express logic. The wrapper core around 'hard block' is designed for handling data from eight lanes of PCI Express bus. Two 8 KB dual port RAM (DPRAM) are built inside the FPGA to handle the data flow to and fro from PCI Express bus. One of the DPRAM input is used by I/O device for writing data. The output port of DPRAM is read by the PCI Express transaction controller and data is transferred to PC via PCI Express. The input port of second DPRAM is connected to PCI Express controller, which transfers data from PC to DPRAM. The output port of this DPRAM is connected to I/O bus wherein the data is finally transmitted. Two samtec I/O connectors are used for I/O interface with one connector providing 24 LVDS (Low Voltage Differential Signalling) inputs and other connector providing 24 LVDS outputs. The I/O speed achieved is 250 MHz maximum using DDR (Dual Data Rate) technique in which the data is acquired at both positive and negative clock edge (clock speed is 125 MHz).

The PCI Express Interface card is a 16 layer PCB (Printed Circuit Board) which is designed with proper impedance matching for all the differential pairs. The simulation is carried out for impedance calculation (prior to board fabrication) for all critical (high speed) signals like clocks, PCI Express lanes etc. Since the board (PCB) has high speed signals, proper layer stacking is done with every alternate layer being a Ground plane.

CONCLUSION

The PCI Express high speed card is completely tested for it's functionality by integrating its device drivers with GUI (Graphic User Interface) written in Microsoft Visual Basic. The maximum data transfer speed of this card is 20 Giga bits per second and can be used for applications like high speed data acquisition, PXI Express 3U size module development etc. Addition of an external ADC/DAC to this card which has LVDS parallel data interface can make this card a complete data acquisition system. These applications are extensively used for Accelerator data acquisition systems as well as RF cavity controls.

REFERENCES

[1] VHDL: Programming By Example by Douglas Perry.
[2] Xilinx Virtex-5 User Guide.
[3] Intel PCI Express Standard.

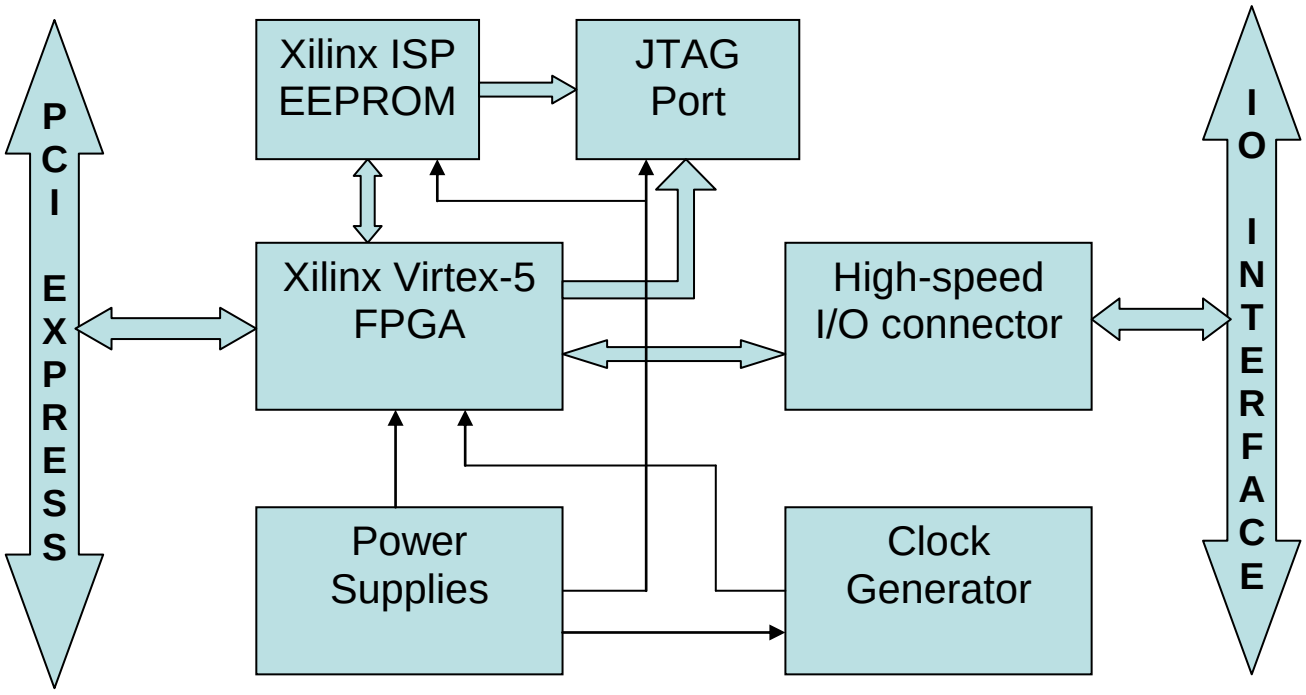

Figure 3: Block diagram of PCI Express Interface Card